Remarks

Thorough examination by the Examiner is noted and appreciated.

The claims have been amended to further clarify Applicants invention.

No new matter has been added. Support for the amended claims are found in the previously presented claims, the Figures and/or the Specification e.g., at:

Paragraph 0022:

Following the second main etch step carried out using at least one of a lower RF source power and RF bias power compared to the first main etch step, an in-situ plasma treatment with one or more inert source gases such as argon, helium, and nitrogen, including mixtures thereof, is carried out for a period of time, for example from about 15 seconds to about 45 seconds with zero RF bias power supplied and with an RF source power of about 50 Watts to about 150 Watts at a pressure of about 2 milliTorr to about 100 milliTorr. It has been found that the inert plasma treatment according to preferred embodiments has the effect of **preventing preferential etching in a subsequent overetch**

process, for example preventing the formation of notches in a p-doped polysilicon gate.

Paragraph 0025:

"Referring to Figure 1G, following the inert gas plasma treatment, an overetch process is carried out to remove remaining portions of the polysilicon layer 18 over the gate dielectric layer 16 including removing polysilicon stringers. In one embodiment, the overetch process is carried out under the same plasma conditions as the second main etching process with no RF bias power applied. Etching with no RF bias power prevents the re-accumulation of charge imbalances at the lower portion of the polysilicon gate during the overetch process."

Claim Rejections under 35 USC 103

1. Claims 1, 2, 4-9, 11-12, 14-19, and 21-22 stand rejected under 35 USC 103(a) as being unpatentable over Lee (5,665,203) in view of Nallan et al. (US 6,902,681) and Grimbergen et al. (6,081,334).

Lee discloses a method for reactive ion etching of a gate electrode using an oxide hardmask layer and a **three step** silicon etching process. Lee discloses disclose etching with CF4 **in a first chamber** to remove any oxide that may have formed on the polysilicon layer during stripping of the resist mask (col 4, lines 31-35). After transfer to a silicon etching chamber a second step is carried out using **HBR/CL2/O2** in a **first silicon etching step** (second etching step)(col4, lines 34-36) and then **HBR/O2** in a third etching step(**second silicon etching step**)(col 4, lines 52-67).

Lee overcomes the problem of etching polysilicon gates **to obtain vertical sidewalls (see col 1, lines 5-9) by oxidizing the sidewalls of the silicon** during the first silicon etch step (second etch step) (col 1, lines 63-66; col 4, lines 38-46) and **stopping a predetermined distance (20 nm) above the gate oxide layer (without exposing the gate oxide), then** removing substantially all CL2 from the etching chamber atmosphere (col 2, lines 1-5; col 4, lines 47-51), and **then etching through a remaining thickness portion of the silicon layer to expose the gate oxide layer** (col 2, lines 1-5; col 4, lines 52-64) **where the second silicon etch step (third etch step) includes an overetch**

process. Lee discloses using low pressure and low power density in the second silicon etch step to expose the gate oxide layer with **no magnetic field enhancement** (col 4, lines 64- col 5, line 3). Lee discloses "a fourth step in the gate etch process" of **dipping in HF to remove oxide residues** from the gate sidewalls (col 5, lines 4-6).

Applicants respectfully point out that Examiner has misinterpreted Lee by asserting that the overetch time included in the **"third step" of the gate etch process** taught by Lee at col 4, lines 52-64 is a fourth RIE etch step. Lee et al., clearly disclose and teach that the **overetch time** is **included** in the **third step of the gate etch process** which is "based on the time for the **final etch step to reach the gate oxide**" (col 4, lines 58-60).

More importantly, **Lee nowhere discloses or suggests performing a plasma treatment following endpoint detection** and exposure of portions of an underlying gate dielectric.

On the other hand, Nallan et al. disclose a method of etching high dielectric constant materials using a halogen gas, reducing gas, and passivating gas chemistry (see Abstract) to

overcome the problem of oxidation of the polysilicon electrode to prevent degradation of the gate structure (col 1, lines 27-45). In one embodiment, the passivating gas (N2) is included in the etch gases of Cl2, CO, and N2 **during etching** of a high-K gate dielectric (**to remove most or all of the gate dielectric to expose the silicon wafer**) and in another embodiment the passivating gas is used **after etching** to **passivate the exposed silicon** (col 1, lines 52-62; col 2, lines 51-65), polysilicon and sidewalls of the gate dielectric **by forming nitride layers over the surface** (col 5, lines 40-56)). The passivating gas N2 may be optionally mixed with one or several inert gases (col 2, lines 48-50).

Nallan et al. generally disclose that a polysilicon gate electrode has previously been etched (prior to etching the high-K gate dielectric) and is used as an etch mask in etching the high-K gate dielectric, **but do not disclose or teach a process for etching a gate electrode** (col 6, lines 34-49).

Nallan et al. generally disclose that **in the two step gate dielectric etch process**; (first etching through the high-K gate dielectric to expose the silicon wafer **and then treating with a passivating plasma using nitrogen** (and one or more inert gases)

that the nitrogen plasma **forms nitride layers** on the exposed portions of the silicon (wafer) and polysilicon (gate electrode) as well as forming an HfON layer on hafnium oxide (high-K gate dielectric) (col 5, lines 40-56) which thereby inhibits oxidation during a subsequent post-etch oxygen plasma cleaning step.

There is no apparent motivation for combining the disparate teachings of Nallan et al., who **teach a gate dielectric etching process** including a plasma treatment process including nitrogen to **form nitride layers** on **exposed silicon or polysilicon** following the gate dielectric etching process, with the method of Lee who discloses a **gate electrode etching process** that **reaches the gate oxide in the final poly silicon-etch step and which is then overetched in the same etch step.**

Moreover, modifying the process of Lee (who teaches a fourth HF dip etch to remove oxide residues on the polysilicon gate) by the process of Nallan, who teaches forming nitride layers in a nitrogen plasma treatment to protect the **exposed silicon** and polysilicon in a subsequent oxygen plasma cleaning process, would make the process of Lee unsuitable for its intended purpose (i.e., HF etch to remove oxide residues on gate electrode sidewall would not remove the nitrided layers formed by the

process of Nallan et al. Moreover, the process of Nallan in carrying out an oxygen plasma cleaning process is inconsistent with the process of Lee in removing oxidation residues along the gate electrode sidewalls.

Examiner argues that Nallan et al. is relied on for the plasma treatment of a gate dielectric. Examiner disregards the fact that the **plasma treatment (including the formation of nitride layers) is carried out following etching through a gate dielectric and exposing the silicon wafer**, a process quite different from etching a gate electrode. Examiner nevertheless argues motivation to modify Lee with Nallan et al. based on the benefits of Nallan et al. (inhibits oxidation of exposed silicon wafer, polysilicon gate electrode and HfON gate dielectric during a subsequent post-etch oxygen plasma cleaning step). However, the formation of such nitride layers by the plasma treatment step of Nallan et al. (prior to etching the gate dielectric) in Lee et al., would form nitride layers on the gate dielectric and over the sidewall oxide residues of Lee, thus interfering with the subsequent HF dip gate electrode sidewall oxide removal step of Lee (one of ordinary skill would understand that HF does not remove nitrides and therefore an oxide underneath the oxide).

Examiner further asserts without any support that the plasma treatment (formation of nitride layers over surface following gate dielectric etching) of Nallan would have the same function as Applicants of "to neutralize an electrical charge imbalance".

However, as pointed out above, Nallan et al. describes a **plasma a treatment to form protective nitride layers** following a gate dielectric etching process. Applicant do not disclose or suggest forming nitride layers (therefore the process of Nallan cannot be the same as Applicants plasma treatment process); further, there is no suggestion to combine the completely different process of gate electrode etching and gate dielectric etching i.e., as explained above, modifying Lee et al. by forming nitride layers following exposure of a gate dielectric following etching a gate electrode would make the subsequent HF dip process to remove oxide residues along gate electrode sidewalls unworkable (**unsuitable for its intended purpose**).

Examiner responds, without any support in the teachings of Lee or Nallan, that **Examiner believes** that the HF dip (to remove oxidation residues on the sidewalls of the gate electrode of Lee) would be beneficial at any stage of fabrication. However, Applicants respectfully note that this is clearly not the case,

as one of ordinary skill would understand that the nitride layers of Nallan over the oxide residues of Lee would make the HF dip to remove the oxide layers of Lee ineffective in the process of Lee **(thus making it unsuitable for its intended purpose)**.

Even assuming *arguendo* the fundamentally different processes of the gate dielectric etching process of Nallan et al. and gate electrode etch process of Lee, are somehow combinable, such combination does not produce Applicants disclosed and claimed invention.

The combined references nowhere teach or suggest performing Applicants **inert gas plasma treatment without material deposition following endpoint detection of an underlying gate dielectric (claim 1) or prior to a subsequent overetch process of said gate dielectric (claim 14)**.

Examiner argues that Nallan is relied on solely for the teaching of treatment of the gate dielectric (a plasma treatment **to form nitride layers** over the exposed silicon substrate, gate electrode and gate dielectric sidewalls following etching of the gate dielectric). However, Applicants do not disclose or claim what Examiner is relying on Nallan for (forming nitride layers).

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).*

In the newly applied reference of Grimbergen et al., the fact that Grimbergen teaches that the use of endpoint detection is well known, does not further help Examiner in producing Applicants invention.

The fact that individual elements in Applicants claims are well known is not a sufficient basis for making out a prima facie case of obviousness.

"The fact that references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references." *Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993).*

2. Claims 3, 10, 13, 20, and 23 stand rejected over Lee and Nallan et al., above, and further in view of Lill et al. (US 6, 284,665).

Applicants reiterate the comments made above, with respect to Lee and Nallan et al.

Lill discloses the use of a **low bias voltage** in the range of 50 to 100 Volts (including no bias power) to avoid ion damage to the gate oxide layer (col 2, lines 46-49) **in a polysilicon etchback (planarization etching) process with an underlying silicon nitride layer.**

The fact that Lill et al. teach typical process conditions for RIE etching of polysilicon selectively to silicon nitride **in**

a polysilicon etchback (flat etch front) process including the use of a low bias Voltage or no bias Voltage, does not further help Examiner in producing Applicants invention or in establishing a *prima facie* case of obviousness.

Even assuming *arguendo*, a proper motivation for combining the disparate teachings of plasma process conditions for completely different etching processes, i.e., a polysilicon etchback (**planarization process**) (Lill et al.) with either a **gate dielectric etching process** (Nallan et al.) or a **polysilicon gate electrode etch process** (Lee) (where an inert gas plasma treatment is neither suggested or disclosed as part of the gate electrode etching process), such further combination with Lill (plasma process conditions for a **polysilicon planarization process**), does not further help Examiner in producing Applicants disclosed and claimed invention.

"Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"The prior art must provide a motivation or reason for the worker in the art, without the benefit of appellant's specification, to make the necessary changes in the reference device." *Ex parte Chicago Rawhide Mfg. Co., 223 USPQ 351, 353 (Bd. Pat. App. & Inter. 1984).*

3. Claims 1-23 stand rejected over Schoenborn (US 5,242,536) in view of Lee et al. (US 5,665,203) and Kim et al. (US 6,620,575) and Winniczek et al (US 6,093,332), Nallan et al. (6,902,681) and Grimbergen et al. (US 6,081,334).

Applicants reiterate the comments made above with respect to Lee et al. and Nallan et al.

Schoenborn teaches that when etching polysilicon with chlorine there is a compromise (tradeoff) between anisotropy and selectivity to oxide etching (i.e., an underlying gate dielectric) (col 2, lines 65-69). Schoenborn also teaches that etching tends to become more isotropic when the underlying oxide (gate dielectric) is exposed (i.e., at endpoint detection when polysilicon residues remain on the surface of the oxide) and that an overetch step is necessary to remove polysilicon residues (col 6, lines 7-19).

Schoenborn teaches an etching chemistry including HBR added to a chlorine containing etching chemistry (Cl2/HBr/He-col 13 lines 60-67) to overcome the problem of isotropic etching (lateral etching of the polysilicon gate electrode including forming notches) during the polysilicon and overetch processes while achieving higher selectivity to the underlying oxide (col 5, lines 29-39). Schoenborn also teaches reducing the RF power (not the RF bias power) in an overetch process to reduce the loss oxide (col 12, lines 25-35, lines 45-48). Schoenborn teaches a 3 step etch process; 1) breakthrough etch (e.g., breakthrough of a native oxide on polysilicon) using He/Cl2 only (see col 5, lines 9-12); 2) a **single main etch step** (using (Cl2/HBr/He) col 13 lines 60-67); and 3) an overetch (removing remaining polysilicon on the underlying oxide) using the same etch chemistry as main etch but with RF power reduced (see col 13, lines 13-16; col 12, lines 54-62).

Schoenborn does not teach several aspects of Applicants invention including the elements in **bold type**:

"A method for improving a polysilicon gate electrode profile to avoid preferential lateral RIE etching **including notching** in a

polysilicon gate electrode etching process comprising the steps of:

providing a semiconductor process wafer comprising a gate dielectric formed over a silicon substrate and a polysilicon layer formed over the gate dielectric;

providing a hardmask layer over the polysilicon layer;

carrying out a first reactive ion etch (RIE) step to etch through a thickness of the hardmask layer to expose the polysilicon layer to form a patterned hard mask for forming a gate electrode;

carrying out a second RIE step to etch through a first thickness portion of the polysilicon layer including an RF source power and an RF bias power;

carrying out a third RIE step to etch through a second thickness portion of the polysilicon layer to endpoint detection to expose portions of an underlying gate dielectric including using **lower ~~etch~~ RF power** compared to the second RIE step, said

lower power selected from the group consisting of a **lower RF source power and a lower RF bias power**; and,

then plasma treating the exposed gate dielectric and polysilicon layer in-situ with an inert gas plasma to neutralize an electrical charge imbalance, said plasma treatment performed without material layer deposition."

Significantly:

Schoenborn does not providing a hardmask layer over the polysilicon layer; (rather Schoenborn teaches that a **native oxide** forms on polysilicon when sitting ex-situ) (see col 12, lines 56-69).

Schoenborn does not disclose or suggest the use of, or level of, an RF bias power.

Schoenborn does not disclose or suggest two main etch (polysilicon etch) steps.

Schoenborn does not disclose or suggest a plasma treatment step (without material layer deposition) following a polysilicon

etch to endpoint.

Schoenborn does not disclose or suggest a plasma treatment step following a polysilicon etch to endpoint and prior to an overetch step (see claim 14).

Schoenborn does not disclose or suggest "A method for improving a polysilicon gate electrode profile to avoid preferential RIE etching including notching in parallel etching of n and p-doped polysilicon gate electrodes" see claim 14.

Examiner relies on Lee et al., above since Lee et al. teach that a polysilicon layer may have both n and p doped regions for forming gate electrodes. It is noted that Lee et al. nowhere recognize the problem of forming notches during the gate electrode etching process, but rather only recognizes that an n-doped gate structure etches faster **anisotropically** (vertically) than a P gate structure using HBr/Cl2 plasma etching chemistries (see col 1, lines 20-29; col 5, lines 30-45). Applicants further note that Schoenborn nowhere recognizes the difference in either anisotropic rates or lateral etch rates in etching P or N doped polysilicon, but only that 'chlorine only' etch chemistry occasionally produces notching (col 5, lines 15-27;col 14, lines

6-15).

Examiner further relies on Lee et al. for the two steps of polysilicon etching. However, the methods of Lee et al. and Schoenborn are fundamentally different in that Lee et al. teaches removing all Cl2 (chlorine) prior to the second polysilicon etching step to expose the underlying oxide gate dielectric. In contrast, Schoenborn **teaches away** from removing all chlorine (e.g., Cl2) but rather teaches adding HBr to chlorine to minimize lateral etching (col 4, lines 3-6; col 9, lines 7-15; col 11, lines 62067). For example, modifying Schoenborn with Lee by removing all chlorine prior to a second polysilicon etch would **change the principle of operation of Schoenborn, as well as make it unsuitable for its intended purpose.**

Moreover, the method of Lee et al. is further different from Schoenborn in that the resist mask of Lee et al. is stripped prior to engaging in the main etch (see col 4, lines 22-27) and where Lee **teaches away** from using a resist mask (see col 2, lines 35-39), while Schoenborn conducts the main etch with the resist in place, which Schoenborn teaches may affect the etching profile by depositing a passivation layer (see Abstract; col 13, lines 60-67).

Examiner again relies on Nallan for the teaching of Applicants claimed inert gas plasma treatment where nitrogen and one or more inert gases are used in a plasma treatment **to form a protective nitride layer following etching of a gate dielectric to expose underlying silicon** as outlined above. Modifying Schoenborn by forming nitride passivation layers prior to an overetch process would also change the principle of operation of Schoenborn who teach that the HBR/Cl2/He etch chemistry should be used in the overetch process to etch an underlying oxide without lateral etching of the polysilicon gate. There is no reason to expect (no teaching in either Schoenborn or Nallan) that formation of nitride layers over the surface (plasma process of Nallan) prior to an overetch process (i.e., over remaining polysilicon over oxide) could be successfully used in the method of Schoenborn, i.e., that the etching chemistry of Schoenborn would now also remove the nitride layers and the remaining polysilicon without significant oxide loss and lateral etching (i.e., the formation of protective nitride layers in the **gate dielectric etching process** of Nallan would be superfluous, and most likely detrimental, in the **gate electrode etching process** of Schoenborn.

Examiner asserts that Schoenborn discloses a polysilicon etch process similar to Lee using minimal etching bias and low power **but is silent on RF source and bias power** in Applicants second etch step or a lower etch power or bias power in Applicants third step.

Examiner therefore looks to Kim et al. who teach a polysilicon etch with RF power where both source and bias and the bias power are adjustably decoupled from the source (see claim 20).

Examiner further looks to Winniczek who teaches a **pulsed RF power** to the chuck which Examiner therefore asserts **includes zero RF power** to reduce polymer deposition on a mask. Applicants assert that one of ordinary skill would not interpret a pulsed RF power to be equivalent to Applicants claim language in light of the Specification "**wherein the step of plasma treating is carried out using zero RF bias power**" as in Applicants claim 2 and 14.

While Applicants do not agree with Examiner broad interpretation of Applicants claim language in light of the Specification, the claims have been amended to read 'without RF bias power' to overcome Examiners broad interpretation.

Even assuming *arguendo*, a motive for combining the disparate and inconsistent teachings of the above references, such combination does not produce Applicants disclosed and claimed invention.

The combined teachings nowhere suggest Applicants claimed gate electrode etching process, including Applicants two polysilicon etching steps, in combination with Applicants **inert gas plasma treatment without material deposition following endpoint detection of a gate dielectric underlying a polysilicon layer in Applicants disclosed and claimed polysilicon etching process.**

Moreover, none of the cited references, singly or in combination, provide Applicants solution to the problem that Applicants have solved by their disclosed and claimed invention (avoiding notching in a gate electrode), but rather teach a different solution (adding HBr to Cl2) (Schoenborn) in a single main etch and overetch to avoid lateral etching and forming an oxide on the gate electrode sidewalls using HBR/Cl2/He/O2 in a first polysilicon etch and then removing all chlorine in a second polysilicon etch (Lee).

"A method for improving a polysilicon gate electrode profile to avoid preferential RIE etching **including notching** in a polysilicon gate electrode etching process".

Moreover, none of the cited references suggest or disclose Applicants polysilicon gate electrode etch process in combination with Applicants inert gas plasma treatment "to neutralize an electrical charge imbalance".

"Finally, the prior art reference (or references when combined) **must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the **reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure.**" *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

"Finally, when evaluating the scope of a claim, every limitation in the claim must be considered. Office personnel may not dissect a claimed invention into discrete elements and then evaluate the elements in isolation. Instead, the claim as a whole must be considered." See, e.g., *Diamond v. Diehr,* 450 U.S. at 188-189, 209 USPQ at 9.

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).*

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).*

In the newly applied reference of Grimbergen et al., the fact that Grimbergen teaches that the use of endpoint detection is well known, does not further help Examiner in producing Applicants invention.

The fact that individual elements in Applicants claims are well known is not a sufficient basis for making out a prima facie case of obviousness.

"The fact that references relied upon teach that all aspects

of the claimed invention were individually known in the art is not sufficient to establish a prima facie case of obviousness without some objective reason to combine the teachings of the references." *Ex parte Levengood, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993).*

Conclusion

The multiple cited references, alone or in combination, fail to produce or suggest Applicants disclosed and claimed invention and therefore fail to make out a *prima facie* case of obviousness with respect to Applicants independent and dependent claims.

Applicants have amended the claims to further clarify their disclosed and claimed invention and respectfully request favorable reconsideration by Examiner.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in

condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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